REMARKS

Claims 1-3, 5-9 and 11-14 are pending in this application. Claims 1-3 and 5-8 stand rejected and claims 11-14 have been withdrawn from consideration and claims 4 and 10 have been canceled without prejudice. By this Amendment, claims 5 and 6 have been amended. The amendments made to the claims do not alter the scope of these claims, nor have these amendments been made to define over the prior art. Rather, the amendments to the claims have been made to improve the form thereof. In light of the amendments and remarks set forth below, Applicants respectfully submit that each of the pending claims is in immediate condition for allowance.

Claims 5 and 6 are amended to overcome the objections raised in the Office Action. Withdrawal of the objection is requested.

Claims 1-3 and 5-8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,523,102 ("Dye") in view of U.S. Patent No. 6,216,485 ("O'Conner"). Applicants respectfully request reconsideration and withdrawal of this rejection.

Applicants note that the claims are directed to a processor comprising a cryptoprocessor, volatile working memory, and address unit which are not present in the combination of Dye and O'Conner.

As shown in Figure 4b of Dye, a computer system having a CPU sub-system 100 memory subsystem 200 and non-volatile memory subsystem 300. See, col. 14, lns. 40-44. In the memory system, an L1 cache 120 and L2 cache 130 are illustrated. The memory subsystem has a memory controller 210 and active pages 220, inactive pages 230 and a compressed cache 240 as well as specific C-DIMM compactor chip. However, Applicants note that Dye is completely silent with respect to the specific internal construction of CPU 110 such as whether CPU 110 has an arithmetic unit for

processing operands or whether the CPU unit additionally has a register memory for storing these operands. CPU 110 and the CPU subsystem are simply illustrated as "black boxes" without any specific details.

It is important to note that it is the specific construction of the CPU that relates to the present claims. However, because Dye is completely silent as to what is behind the CPU or the CPU subsystem memory 120 and 130, the assertions with respect to Dye fail to disclose the assertions set forth in the Office Action.

With respect to the Office Action, Applicants note that there is a cryptocoprocessor explicitly recited in the claims. However, the Office Action points to the computer system at items 100, 200, and 300. However, a cryptocoprocessor or generally a processor is different from a computer system. At best, one might assert that the CPU 110 corresponds to the processor. The Office Action further points to system memory 200 in Figure 4b as the register memory. However, the term "register memory" is used for indicating the specific registers within a CPU which are specifically linked to the arithmetic unit and particularly used for storing the operands which are processed by the arithmetic unit. However, in contrast to the assertion of the Office Action, it would be improper to say that a RAM working memory of a computer is the register memory. Instead, RAM working memory is completely different from the specific register memory within the processor.

The Office Action improperly equates the register memory configuration unit with the virtual memory manager 620. However, this device does not care at all about any specific register memory within the CPU 110. In fact, this feature is not addressed in the Office Action. The specific feature regarding the usage of a certain register memory space for operands in which portion of this register memory is not used by operands is not present. Virtual memory manager 620 discussed at col. 6, lns. 38-65 only cares for the cooperation of the memory subsystem and the non-volatile disk

system 300. Specifically, some pages in the memory subsystem can be compressed and buffered in the disk system 300. However, it can easily be seen that this is not related to specific registries within the CPU.

With respect to the volatile external working memory, the Office Action points to item 500 in Figure 4a. However, the items referred to in the Office Action specifically at col. 15, lns. 9 and 10, are not within item 15 in Figure 4a but within the memory subsystem 200. Applicants respectfully submit that block 500 does not have a specific connection to blocks 100, 200, or 300 in Figure 2b since Figure 4a is a completely different Figure. Importantly, the compactor chip 250 is also part of the memory subsystem only.

With respect to the limitation that the register memory space is physically disposed within the processor, the Office Action points to a main memory in the processor without any specific indication. However, the memory subsystem 200 is not located within the CPU 110 but located outside of the CPU 110.

The conclusion in the Office Action that the memory space is mapped into the working memory is incorrect since the compressed cache pg. 240 is not a register memory but is part of the straight forward working memory. This working memory could at best be compared to other XRAM 32 which is, for example, illustrated in Figure 2 of the present application.

With respect to the address unit, the Office Action points to col. 19 and col. 20. However, this process does not relate to what happens within the CPU 110 but only addresses matters regarding the memory subsystem which, as discussed above, is not a register memory.

In numbered paragraph 6, the Office Action acknowledges that the feature of making available non-used register memory space for other data is not disclosed in

Dye. However, it is the address unit feature which is based on this free-register space. Specifically, the address unit as defined in claim 1 addresses this free-register memory space in the same way as the external working memory. Therefore, Dye fails to disclose making non-used register space available for other data than Dye cannot also disclose the address unit as defined in claim 1.

Applicants note that the citing of O'Conner fails to cure the deficiencies noted in Dye above.

Initially, Applicants note that the randomly accessible storage 810 which is included in the stack management unit 150 in Figure 1 of Dye is not the register memory for storing operands explicitly recited in the claims.

First, the stack is a randomly accessible storage 810 and is not outlined in O'Conner as the register memory. Instead, O'Conner teaches register 144 as stated in col. 20, ln. 30. Thus, the stack 810 is not a register memory.

Second, the constant 814 is constantly used for commonly used constants such as specify job of virtual machine instructions and the like. See, col. 21, lns. 3-6. Thus, the constant pool is not used for storing operands. Operands are never written into the constant pool 814.

In contrast, the register memory configuration unit explicitly recited in claim 1 configures the register memory such that memory register space not needed by operands is made available for data other than the operands. Because the constant pool 814 is never used for operands, O'Conner has no need to have a register memory configuration unit designed to configure the register memory. The constant pool 814 is always used for data other than operands irrespective of how many registers are populated by operands for a specific operation. Thus, O'Conner fails to disclose the register memory configuration unit.

Applicants note that while Figure 11 indicates that an output of the constant pool 814 as being an operand, is only disclosed in col. 23 for a specific embodiment. Thus, a processor either has the constant pool 814 for operands or it does not. There is no configuration unit which would change a processor for one application to a processor for another application.

O'Conner is also completely silent as to the address unit specifically that the register memory space not assigned to operands is addressed in the same way as the external working memory being physically disposed outside the processor.

Applicants note that memory 810 is not a register memory. Further, the memory area 814 is not at all addressed in the same way as an external memory connected to the IO BUS and memory interface unit in Figure 1. Instead, O'Conner teaches that there is in one embodiment in which portion 814 has operands and there is another embodiment in which 814 does not have operands but has certain constants. In the embodiment in which the constant pool 814 has constants, there is no indication that the constant pool is addressed in the same way as external memory. Thus, as illustrated in Figure 2 of the present application and explicitly recited in the claims, the register memory is completely mapped into the straight forward memory map of the whole system so that each device can use this memory and this feature is not at all disclosed in O'Conner. Instead, when the constant pool is not used for operands but for constants, this pool is not addressed in the same way as the external memory by an address unit. Specifically, the IO BUS and memory interface unit does not have any connection to the stack management unit 150. However, such a connection and specific address would have to be there for the rejection set forth in the Office Action to be proper. Thus, for at least the reasons discussed above, the combination of Dye and O'Conner fail to anticipate the pending claims.

Applicants have responded to all of the rejections and objections recited in the Office Action. Reconsideration and a Notice of Allowance for all of the pending claims are therefore respectfully requested.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If the Examiner believes an interview would be of assistance, the Examiner is welcome to contact the undersigned at the number listed below.

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Respectfully submitted,
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